

REMARKS/ARGUMENTS

This letter is responsive to the Office Action dated August 14, 2002. This response is accompanied by a request for a one-month extension of time. Accordingly, this response is timely filed.

By this response, claims 1-3, 7-12, 16, 21-22, 27-30, 34-67, 70-71, 76, 82-85, 90 and 96-98 have been amended. All of these amendments have been done without prejudice. In addition, Figures 3, 5, 6, 8, 10, 11 and 14-17 and various paragraphs in the specification have been amended. The Applicant submits that no new matter has been added by any of these amendments.

In the Office Action, the Examiner objected to the specification because the phrase "diode-or'd" should be correctly indicated as --diode-OR'd-- on page 20, line 24 of the application as filed. In response, the Applicant has amended this portion of the specification to comply with the Examiner's suggestions. The Applicant has also found additional instances of the phrase "diode-or'd" in the application as filed which have now been replaced with --diode-OR'd-- as amended herein. These instances occur on: a) page 19, line 21, b) page 21, line 15, c) page 24, line 23, d) page 28, line 10, e) page 29, line 14, and f) page 40, line 18 of the application as filed.

The Examiner also objected to the specification for failing to provide proper antecedent basis for the specific impedance values disclosed in claims 31, 32, 68 and 69. These claims specify that the first impedance coupling the first isolation amplifier to the first input terminal is greater than 50 k Ω (claims 31 and 68) or is equal to or greater than 100 k Ω (claims 32 and 69). The Examiner stated that these impedance values must be disclosed in the specification.

In response, the Applicant has amended the specification on page 42, lines 21 to 23 of the application as filed to state that "resistors 822 and 826 may have a

resistance greater than 50 k Ω such as 100 k Ω or more and resistor 824 may have a resistance of 1 M Ω ".

In the Office Action, the Examiner rejected claims 21, 22, 58 and 59 under 35 USC s. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The Examiner stated that it is unclear which "combining circuit" is a pair of diodes, since the "combining circuit" as stated in claim 21/58 appears to be summer (368) of Figure 4 and not a pair of diodes (360a and 360b).

The Applicant reminds the Examiner of a telephone interview with Bhupinder Randhawa on August 8, 2002 in which the Examiner stated that the language "diode OR'ing" in claim 22 and combining circuit in claim 21 is not acceptable since there is confusion with the word "combining" in claim 19. The Examiner stated that the "combining circuit" in claim 21 should be renamed and that the language here refers to Figure 4 and page 20 of the specification as filed in which diodes 360A and 360B are used to effectively select the higher of the two compensated input signals 340A and 340B. The Examiner also stated that the language "diode OR'd" should be used in these claims to comply with the language that is used in the description.

In response, the Applicant has amended claims 21 and 58 to recite a magnitude comparing circuit (rather than a combining circuit) for comparing (rather than combining) the first and second compensated input signals and providing the compensated input signal with a magnitude corresponding to the higher magnitude of the first and second compensated input signals.

The Applicant has also amended claims 22 and 59 to recite that the magnitude comparing circuit (rather than the combining circuit) is a pair of diodes wherein the first and second compensated input signals are diode OR'd for generating the

compensated input signal. Accordingly, the Applicant respectfully submits that claims 21, 22, 58 and 59 are now allowable.

In the Office Action, the Examiner indicated that claims 1-20, 22-57 and 60-98 are allowed. However, the Examiner objected to claims 1, 2, 7-12, 22, 27, 29, 30, 34-67, 70, 82-84, 89, 90 and 96-98 based on informalities related to antecedents. In response, the Applicant has made the following amendments outlined below to the identified claims to correct informalities due to antecedents as well as to correct typographical errors. The Applicant has also made several other typographical corrections to the claims as described below. The Applicant submits that none of these amendments introduce new subject matter.

-Claim 1, line 6, "input terminal" has been corrected to read --first input terminal--; "input signal" has been corrected to read --first input signal--; and "output terminal" has been corrected to read --first output terminal--

-Claim 1, line 7, "the output" has been corrected to read --the first output--.

-Claim 1, line 17, "the input" has been corrected to read --the first input--.

-Claim 1, line 19, last occurrence of "the" has been corrected to read --a--.

-Claim 1, line 26, "the input" has been corrected to read --the first input--.

-Claim 1, line 27, "the" has been corrected to read --a--.

-Claim 1, line 28, "the slew rate" has been corrected to read --a slew rate--.

-Claim 2, line 12, "input compensation circuit" has been corrected to read --input signal compensation block--.

-Claim 2, line 14, "said input" has been corrected to read --said first input--.

-Claim 2, line 17, "compensated circuit" has been corrected to read --compensated signal-- to correct a typographical error.

-Claim 2, line 20, "compensated circuit" has been corrected to read --compensated signal-- to correct a typographical error.

-Claim 3, line 24, "selected" has been removed to correct a typographical error.

-Claim 7, line 6, "input offset block" has been corrected to read --offset block--.

-Claim 7, line 8, "input signal" has been corrected to read --first input signal--.

-Claim 8, line 11, "signal" has been inserted after "input".

-Claim 8, line 13, "first amplifier" has been corrected to read --first signal amplifier--.

-Claim 9, line 17, the word "first" has been deleted.

-Claim 9, line 18, "signal" has been changed to --circuit-- to correct a typographical error.

-Claim 10, line 25, "(ii)" has been changed to --(iii)--; and "the" has been inserted before "switch" to correct typographical errors.

-Claim 10, line 26, "main" has been inserted after "unfiltered".

-Claim 11, line 29, "the EMI" has been corrected to read --EMI--.

-Claim 12, page 54, line 1, "the" has been changed to --a--.

-Claim 12, page 54, line 12, "(iv)" has been changed to --(vi)-- to correct a typographical error.

-Claim 16, lines 25 and 26, "unfiltered power signal" has been changed to --unfiltered main power signal--.

-Claim 21, line 19, the word "block" has been added after compensation to correct a typographical error.

-Claim 27, line 24, "a" has been changed to --an--.

-Claim 27, page 57, line 1, "the" has been changed to --a--.

-Claim 28, line 7, "the first amplifier" has been changed to --the first signal amplifier--.

-Claim 29, line 12, "the" has been changed to --a--.

-Claim 29, line 14, "said output signal" has been changed to --said first output signal--.

-Claim 29, line 16, "said output signal" has been changed to --said first output signal--.

-Claim 30, line 22, "node" has been changed to --terminal--.

-Claim 30, line 24, "said input" has been changed to --said first input--.

-Claim 30, line 30, "amplification factor" has been changed to --first amplification factor--.

-Claim 30, lines 30, 31, "amplification factor" has been changed to --second amplification factor--.

-Claim 34, lines 14, 15, "the input" has been changed to --the first input--.

-Claim 34, line 15, "the input" has been changed to --the first input--.

-Claim 34, line 15, "the output" has been changed to --the first output--.

-Claim 34, line 16, "the output" has been changed to --the first output--.

-Claim 34, line 26, "the input" has been changed to --the first input--.

-Claim 34, page 59, line 1, "the input signal" has been changed to --the first input signal--.

-Claim 34, page 59, line 2, "the" has been changed to --a--.

-Claim 34, page 59, line 3, "the slew rate" has been changed to --a slew rate--.

-Claim 34, page 59, line 7, "first transient control signal" has been changed to --first digital transient control signal--.

-Claim 34, page 59, line 9, "second transient control signal" has been changed to --second digital transient control signal--.

-Claim 34, page 59, line 20, "signal" has been changed to --circuit--.

-Claim 34, page 59, lines 20, 21, "second transient control circuit" has been changed to --second digital transient control signal--.

-Claim 34, page 59, line 23, "second transient control signal" has been changed to --second digital transient control signal--.

-Claims 35-65, the preamble "the power supply circuit of claim" has been changed to read --the first power supply circuit of claim--.

-Claim 35, line 2, "first transient control signal" has been changed to --first digital transient control signal--.

-Claim 36, line 7, "second transient control signal" has been changed to --second digital transient control signal--.

-Claim 37, line 13, "a fast release block" has been changed to --a fast attack block--.

-Claim 39, line 24, "a" has been inserted after "to".

-Claim 40, line 6, "second transient control signal" has been changed to --second digital transient control signal--.

-Claim 42, line 19, "circuit" has been changed to --block--.

-Claim 42, line 21, "said input signal" has been changed to --said first input signal--.

-Claim 42, line 24, "circuit" has been changed to --signal-- to correct a typographical error.

-Claim 42, line 27, "circuit" has been changed to --signal-- to correct a typographical error.

-Claim 43, line 31, "selected" has been deleted to correct a typographical error.

- Claim 47, line 13, the word "input" has been deleted.
- Claim 47, line 15, "the input signal" has been changed to --the first input signal--.
- Claim 48, line 18, "first input compensation block" has been changed to --first input signal compensation block--.
- Claim 48, line 20, "first amplifier" has been changed to --first signal amplifier--.
- Claim 49, line 24, "first" has been deleted.
- Claim 50, line 30, "the power source" has been changed to --the main power source--.
- Claim 50, page 63, line 2, "unfiltered power signal" has been changed to --unfiltered main power signal--.
- Claim 51, line 4, "the" has been changed to --a--.
- Claim 51, line 5, "the EMI" has been changed to --EMI--.
- Claim 52, line 9, "the peak" has been changed to --a peak--.
- Claim 52, line 12, "the rate" has been changed to --a rate--.
- Claim 53, line 19, "unfiltered power signal" has been changed to --unfiltered main power signal--.
- Claim 55, line 25, "first amplifier" has been changed to --first signal amplifier--.
- Claim 55, line 27, "first amplifier" has been changed to --first signal amplifier--.
- Claim 55, lines 30 and 31, "to the adjusted compensated input signal and compensated" has been changed to --to a difference between the adjusted compensated input signal and the compensated-- to correct an inadvertent omission.

-Claim 58, line 8, "second amplifier" has been changed to --second signal amplifier--.

-Claim 58, line 9, "the power terminal" has been changed to --the first power terminal--.

-Claim 58, line 12, "from" has been changed to --block--.

-Claim 61, line 27, "a" has been changed to --an--.

-Claim 62, line 30, "the power terminal" has been changed to --the first power terminal--.

-Claim 64, line 10, "first amplifier" has been changed to --first signal amplifier--.

-Claim 64, line 12, "first amplifier" has been changed to --first signal amplifier--.

-Claim 64, line 17, "providing a" has been changed to --providing an--.

-Claim 64, line 22, "the power terminal" has been changed to --the first power terminal--.

-Claim 64, line 23, "the power" has been changed to --the first power--.

-Claim 64, line 25, "the difference" has been changed to --a difference--.

-Claim 65, line 30, "first amplifier" has been changed to --first signal amplifier--.

-Claim 66, line 4, "the same structure" has been changed to --a same structure--.

-Claim 66, line 6, "said output signal" has been changed to --said first output signal--.

-Claim 66, line 8, "said output signal" has been changed to --said first output signal--.

-Claim 67, line 14, "node" has been changed to --terminal--.

-Claim 67, line 17 "said input" has been changed to --said first input--.

-Claim 67, line 23, "the amplification" has been changed to --the first amplification--.

-Claim 67, lines 23 and 24, "the amplification" has been changed to --the second amplification--.

-Claim 70, line 6, "power signal" has been changed to --total power signal--.

-Claim 70, line 7, "compensated signal" has been changed to --compensated input signal--.

-Claim 70, line 7, "the power" has been changed to --the total power--.

-Claim 70, line 13, "the rate" has been changed to --a rate--.

-Claim 70, line 16, "the threshold" has been changed to --the transient threshold--.

-Claim 70, line 16, "the maximum" has been changed to --a maximum--.

-Claim 70, line 17, "supply" has been changed to --signal-- to correct a typographical error.

-Claim 70, line 20, "a transient condition" has been changed to --the transient condition-- since a transient condition has been previously introduced.

-Claim 71, line 24, "offset the" has been changed to --offset to the-- to correct a typographical error.

-Claim 76, line 14, "the amplifier" has been changed to --the signal amplifier--.

-Claim 82, line 2, "the amplifier" has been changed to --the signal amplifier--.

-Claim 83, line 5, "the amplifier" has been changed to --the signal amplifier--.

-Claim 84, lines 11 and 12, "the power signal" has been changed to --the total power signal--.

-Claim 84, line 13, "the compensated signal" has been changed to --the compensated input signal--.

-Claim 84, lines 13 and 14, "the power signal" has been changed to --the total power signal--.

- Claim 84, line 19, "the rate of change" has been changed to --a rate of change--.
- Claim 84, line 22, "the threshold" has been changed to --the transient threshold--.
- Claim 84, line 22, "the maximum" has been changed to --a maximum--.
- Claim 84, line 23, "supply" has been changed to --signal-- to correct a typographical error.
- Claim 85, line 29, "offset the" has been changed to --offset to the-- to correct a typographical error.
- Claim 90, line 18, "the amplifier" has been changed to --the signal amplifier--.
- Claim 96, line 6, "the amplifier" has been changed to --the signal amplifier--.
- Claim 97, line 9, "the amplifier" has been changed to --the signal amplifier--.
- Claim 98, lines 14 and 15, "the input terminal" has been changed to --the first input terminal--.
- Claim 98, line 15, "the input signal" has been changed to --the first input signal--.
- Claim 98, line 15, "the output terminal" has been changed to --the first output terminal--.
- Claim 98, line 16, "the output signal" has been changed to --the first output signal--.
- Claim 98, line 26, "the input signal" has been changed to --the first input signal--.
- Claim 98, line 29, "the power level" has been changed to --a power level--.
- Claim 98, line 30, "the summer" has been changed to --the first summer--.
- Claim 98, line 31, "second" has been changed to --first-- to correct a typographical error.
- Claim 98, page 72, line 6, "the input signal" has been changed to --the first input signal--.
- Claim 98, page 72, line 7, "a second" has been changed to --the second--.
- Claim 98, page 72, line 9, "the power" has been changed to --a power--.

-Claim 98, page 72, line 10, "the summer" has been changed to --the second summer--.

-Claim 98, page 72, line 14, "the input signal" has been changed to --the first input signal--.

-Claim 98, page 72, lines 15 and 16, "the rate of change" has been changed to --a rate of change--.

-Claim 98, page 72, line 16, "the slew rate" has been changed to --a slew rate--.

However, upon reviewing the claims as filed, the Applicant has not made the following amendments that were suggested by the Examiner because changes do not have to be made for the reasons specified below.

-Claim 1, page 52, line 3, the suggested amendment was not made since the feature "transient signal" is correctly referred to

-Claim 1, page 52, line 4, the suggested amendment was not made since the feature "transient signal" is correctly referred to

-Claim 8, lines 13, 14, the suggested amendment was not made since it is the first output signal of the power amplifier that is properly referred to.

-Claim 29, line 16, the suggested amendment was not made since "said output" should not be --said second output-- but rather --said first output-- as amended herein and described above.

-Claim 38, line 18, the suggested amendment was not made since "attack" is the correct term and the term "release" was incorrectly introduced in claim 37; rather claim 37 has been amended herein as described above.

-Claim 66, line 8, the suggested amendment was not made since "said output" should not be --said second output-- but rather --said first output-- as amended herein and described above.

-Claim 70, line 15, the suggested amendment was not made since the phrase "the rate of change" refers to the phrase "a rate of change" on line 13 of claim 70.

-Claim 70, line 17, the suggested amendment was not made since the "main power supply " should be the "main power signal" and this element has already been introduced into claim 70.

-Claim 89, line 15, the suggested amendment was not made since "a slew rate" was introduced in claim 84.

-Claim 98, line 31 to page 72, line 1, the suggested amendment was not made since "the second error signal" should be "the first error signal" which was introduced in paragraph (c) of claim 98.

The Examiner also stated that the lengthy specification was not checked to the extent necessary to determine the presence of all possible minor errors and that the Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware in the specification.

In response, the Applicant has checked the specification and corrected the typographical errors of which the Applicant is aware. The details of the correction of the typographical errors are provided in the attached page captioned "**Version with markings to show changes made.**" The Applicant has also amended the Summary of the Invention section to remove claim language (i.e. the word "said") and to insert paragraphs that correspond with the independent claims of the application as filed, and in some cases, as corrected herein.

The Applicant has also amended Figures 3, 5, 6, 8, 10, 11, and 14 to 17 due to either the omission or incorrect labeling of some reference numbers as well as the omission of some elements. The Applicant submits marked up versions of the Figures to show the amendments as well as clean copies of the amended Figures to be used as Formal Figures.

In particular, the Applicant has amended Figure 3 to label the control circuit with reference numeral 284 and to correctly label the control signal with reference label 290 rather than reference label 242. The Applicant has amended Figure 5

to correctly label the output signals with reference labels 332a and 332b rather than reference labels 322a and 322b. The Applicant has also amended Figure 6 to add the error signal 239.

In addition, the Applicant has amended Figure 8 to label the switch with reference label 224 and to include the error signal 239 and the rectified signal 240. The Applicant has amended Figure 10 to label the switch with reference label 224. The Applicant has amended Figure 11, to indicate that there is a capacitor C_9 located between the capacitor C_2 and the resistor R_{10} . Support for this amendment is in paragraph 114 of the application as filed. In addition, the base of transistor Q_9 has been connected between resistors R_{13} and R_{14} . Support for this amendment is in paragraph 116 of the application as filed.

The Applicant has amended Figure 14 to replace reference label 705b with 705a and 709 with 709a respectively. The Applicant has also labeled the second bridge amplifier at the bottom of Figure 14 with reference label 709b. The Applicant has also amended Figure 15 to include reference label 204 for the amplifier connected to node 206, as well as reference labels 849a and 849b for the inputs of amplifier 820. The Applicant has also added reference label 812 to represent the chassis ground connected to capacitor 828, the positive input of amplifier 830 and the resistor 234. Support for these reference label amendments is in paragraphs 140-149 on pages 41-43 of the application as filed.

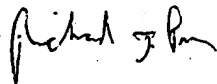
The Applicant has amended Figure 16 to correct incorrect reference labels. In particular, the reference labels 905, 146 and 137 have been replaced with the reference labels 906, 142 and 937 respectively. Support for these reference label amendments is in 150-155 on pages 44-46 of the application as filed. In addition, the Applicant has amended Figure 17 to add reference numeral 1044 to the capacitor connected to node 1054 and to add reference numeral 1040 to the diode that is connected to node 1056. Support for these reference label amendments is in paragraph 159 on page 47 of the application as filed.

Attached hereto is a marked-up version of the changes made to the description, figures and claims by the current amendment. The attached page is captioned: **Version with markings to show changes made.**

Conclusion

In view of the foregoing comments, it is respectfully submitted that the application is now in condition for allowance and the applicant respectfully requests a timely Notice of Allowance be issued in this case. If the Examiner has any further concerns regarding the language of the claims or the applicability of the prior art, the Examiner is respectfully requested to contact the undersigned at 416-957-4686.

Respectfully submitted,
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TRO / cec

"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

In the Drawings:

Figures 3, 5, 6, 8, 10, 11, and 14 to 17 have been amended as shown in the "Version With Markings To Show Changes Made" section.

In the Description:

Please amend the paragraph beginning on page 3, line 23 as follows:

In a first embodiment, the present invention provides: a power amplifier for receiving an input signal at an input terminal and producing an output signal at an output terminal, ~~said~~the output signal corresponding to ~~said~~the input ~~terminal~~signal, ~~said~~the power amplifier having a first power supply circuit comprising: an amplifier coupled to ~~said~~the input terminal for receiving ~~said~~the input signal and coupled to ~~said~~the output terminal for providing ~~said~~the output signal, ~~said~~the amplifier having a power input terminal for receiving a power input signal; a switching regulator coupled to ~~said~~the power input terminal for providing a switching power signal to ~~said~~the amplifier, wherein ~~said~~the switching power signal forms a first part of the power input signal; a linear regulator coupled to ~~said~~the power input terminal, ~~said~~the linear regulator being selectively engageable to provide a linear power signal to ~~said~~the amplifier, wherein ~~said~~the linear power signal forms a second part of ~~said~~the power input signal; an input signal processing circuit coupled to ~~said~~the input terminal for receiving ~~said~~the input signal and for providing a rectified signal indicating the amount of power required by ~~said~~the amplifier; a control circuit coupled to ~~said~~the input signal processing circuit and to ~~said~~the power input terminal for controlling ~~said~~the switching power signal and ~~said~~the linear power signal in response to an error signal corresponding to a ~~between~~ ~~said~~the rectified signal and ~~said~~the power

input signal; a linear regulator control circuit coupled to ~~said~~the input signal processing circuit for receiving ~~said~~the rectified signal and coupled to ~~said~~the linear regulator for controlling the engagement of ~~said~~the linear regulator in response to ~~said~~the rectified signal.

Please amend the paragraph beginning on page 4, line 14 as follows:

In a second embodiment, the present invention provides a power amplifier for receiving an input signal at an input terminal and producing an output signal at an output terminal, ~~said~~the output signal corresponding to ~~said~~the input terminal, ~~said~~the power amplifier having a first power supply circuit comprising: an EMI isolation circuit coupled to ~~said~~the input terminal for receiving ~~said~~the input signal and to an internal input node for providing an EMI-decoupled signal corresponding to ~~said~~the input signal; an amplifier coupled to ~~said~~the input terminal for receiving ~~said~~the input signal and coupled to ~~said~~the output terminal for providing ~~said~~the output signal, ~~said~~the amplifier having a power input terminal for receiving a power input signal; a switching regulator coupled to ~~said~~the power input terminal for providing a switching power signal to ~~said~~the amplifier, wherein ~~said~~the switching power signal forms a first part of the power input signal; a linear regulator coupled to ~~said~~the power input terminal, ~~said~~the linear regulator being selectively engageable to provide a linear power signal to ~~said~~the amplifier, wherein ~~said~~the linear power signal forms a second part of ~~said~~the power input signal; an input signal processing circuit coupled to ~~said~~the internal input node for receiving ~~said~~the EMI-decoupled signal and for providing a rectified signal indicating the amount of power required by ~~said~~the amplifier; a control circuit coupled to ~~said~~the internal input signal processing circuit and to ~~said~~the power input terminal for controlling ~~said~~the switching power signal and ~~said~~the linear power signal in response to an error signal corresponding to a ~~between~~said ~~said~~the rectified signal and ~~said~~the power input signal; a linear regulator control circuit coupled to ~~said~~the input signal processing circuit for receiving

said ~~the~~ rectified signal and coupled to said ~~the~~ linear regulator for controlling the engagement of said ~~the~~ linear regulator in response to said ~~the~~ rectified signal.

Please add the following paragraphs beginning on page 5, line 6 as follows:

A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, ~~said the first output signal corresponding to said the first input signal~~, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising: a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level; a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal; a summer coupled to the first input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and a power level of the total power signal; a control circuit coupled to the summer for receiving the error signal and for providing a first control signal and a second control signal in response to the error signal, wherein the first control signal corresponds to a target main power signal level and the second control signal corresponds to a target transient power signal level; a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when a rate of change in a slew rate of the compensated input signal exceeds a selected transient threshold; a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the

transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists; wherein the control circuit provides the first and second control signals such that the target main power signal level is equal to or higher than the target transient power signal level and wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, the first output signal corresponding to the first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and the power amplifier having a first power supply circuit comprising: a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level; a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal; a summer coupled to the first input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and the power level of the total power signal; a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when a rate of change in a slew rate of the compensated input signal exceeds a selected transient threshold; a first transient control circuit coupled to the transient detect block for providing first and second digital transient control signals, wherein the first digital transient control signal indicates the occurrence of a transient condition for a first time period in response to the transient signal and wherein the second digital transient control signal indicates the occurrence of a transient condition for a second time period in response to the transient signal, and wherein the second

time period is longer than the first time period; a control circuit coupled to the summer for receiving an amplified error signal for providing a first control signal in response to the amplified error signal; a signal combining block for combining the first control signal and the first transient control signal to provide a main power supply control signal; a selectively engageable second transient control circuit coupled to the first transient control circuit for receiving the second digital transient control signal and for temporarily increasing the magnitude of the error signal, wherein the second transient control circuit is engaged and disengaged in response to the second digital transient control signal, the second transient control circuit including a feedback amplifier coupled between the summer and the control circuit to provide the amplified error signal, the feedback amplifier being operative at all times; and a main power supply for providing a main power signal at the first power terminal in response to the main power supply control signal; wherein the total power signal corresponds to the main power signal.

A method of supplying a total power signal to a signal amplifier, comprising: receiving an input signal; producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target power level for the total power signal; comparing the compensated input signal to a reduced version of the total power signal to produce an error signal; providing first and second control signals in response to the error signal; providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal; comparing a rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the transient threshold, the transient threshold corresponding to a maximum slew rate of the main power signal; and engaging a transient power supply to provide a transient power signal in response to the second control signal, when the transient signal indicates the transient condition, the transient power signal being a second part of the total power signal.

A method of supplying a total power signal to a signal amplifier, comprising: receiving an input signal; producing a compensated input signal

corresponding to the input signal, the compensated input signal defining a target power level for the total power signal; comparing the compensated input signal to a reduced version of the total power signal to produce an error signal; providing first and second control signals in response to the error signal; providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal; comparing a rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the transient threshold, the transient threshold corresponding to a maximum slew rate of the main power signal; and in response to a transient condition, temporarily engaging the switching regulator with a 100% duty cycle for a first time period and temporarily elevating the error signal for a second time period.

A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, the first output signal corresponding to the first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and the power amplifier having a first power supply circuit comprising: a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level; a main power signal compensation block for receiving a main power signal and for providing a compensated main power signal corresponding to the main power signal; a first summer coupled to the first input signal compensation block and to the main power signal compensation block for providing a first error signal corresponding to a difference between the target power level and a power level of the main power signal; a first control circuit coupled to the first summer for receiving the first error signal and for providing a first control signal in response to the first error signal, wherein the first control signal corresponds to a target main power

signal level; a total power signal compensation block for receiving the total power signal and for providing a compensated total power signal corresponding to the total power signal; a second summer coupled to the first input signal compensation block and to the total power signal compensation block for providing the second error signal corresponding to a difference between the target power level and a power level of the total power signal; a second control circuit coupled to the second summer for receiving the second error signal and for providing a second control signal in response to the second error signal, wherein the second control signal corresponds to a target transient power signal level; a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when a rate of change in a slew rate of the compensated input signal exceeds a selected transient threshold; a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists; wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

Please amend the paragraph beginning on page 5, line 9 as follows:

Figure 1 is a block diagram of a first embodiment of a power amplifier according to the present invention;

Figure 2 illustrates a second embodiment of a power amplifier according to the present invention;

Figure 3 illustrates a third embodiment of a power amplifier according to the present invention;

Figure 4 illustrates a fourth embodiment of a power amplifier according to the present invention;

Figure 5 illustrates ~~a~~ illustrates the headroom between a power supply signal of the power amplifier of Figure 4 and a pair of input signals to that power amplifier;

Figure 6 illustrates a fifth embodiment of a power amplifier according to the present invention;

Figure 7 illustrates the relationship between a power signal produced by a switching regulator and a low voltage power supply of the power amplifier of Figure 6;

Figure 8 illustrates a sixth embodiment of a power amplifier according to the present invention;

Figure 9 illustrates a pulse of a power signal produced by a resonant switching regulator of the power amplifier of Figure 8;

Figure 10 illustrates a seventh embodiment of a power amplifier according to the present invention;

Figure 11 illustrates part of the feedback control circuit of the power amplifier of Figure 10;

Figure 12 illustrates another part of the feedback control circuit of the power amplifier of Figure 10;

Figure 13 is a timing diagram illustrating the production of PDM control signal of the power amplifier of Figure 10;

Figure 14 illustrates an eighth embodiment of a power amplifier according to the present invention;

Figure 15 illustrates an input filtration circuit according to the present invention which may be used with a power amplifier;

Figure 16 is a block diagram of a ninth embodiment of a power amplifier according to the present invention;

Figure 17 illustrates a tenth embodiment of a power amplifier according to the present invention; and

Figure 18 is a timing diagram illustrating the operation of the power amplifier of Figure 17.

Please amend the paragraph beginning on page 7, line 5 as follows:

Input compensation block 105 is coupled to input terminal 102 to receive input signal 130 and to provide a compensated input signal 140 at a terminal 117. Amplifier 104 receives a power signal V_i from a positive power terminal 136. Power signal V_i is the sum of a power signal V_s provided by main power supply 118 and a power signal V_t provided by transient power supply 123. The voltage of power signal V_i is equal to the greater of the voltages of power signals V_s and V_t . Output power signal compensation block 135 is coupled to positive power terminal 136 and provides a compensated power signal V_{tr} , which has a range comparable to that of compensated input signal 140. Summer 137 compares compensated input signal 140 to compensated power signal V_{tr} and provides an error signal 139. ~~Input compensation block 105 and output power signal compensation block 135 are configured to produce~~

Please amend the paragraph beginning on page 8, line 14 as follows:

During this finite time, power amplifier 100 enters a "transient operation" and transient power supply 123 is engaged to provide power signal V_t to amplifier 104. Transient detection block 119 monitors compensated input power signal 140 at terminal 117 and, when a transient that exceeds a selected threshold occurs in input signal 130, transient detection block 119 enables transient power supply 123. The threshold is selected ~~to~~ so that transient power supply 123 will be engaged when main power supply 118 is unlikely to be able to provide power signal V_s with a magnitude approximately equal to V_{target} . The selection of the threshold will depend on the slew rate of main power supply 118.

Please amend the paragraph beginning on page 13, line 3 as follows:

When the frequency of input signal 230 is relatively low, power signal V_s will follow the waveform of output signal 232, with some headroom. As the slew

rate of input signal 230 rises, main power supply 218 may be unable to change the magnitude of power signal V_s sufficiently quickly to follow output signal 232, which will have a correspondingly high slew rate. (Main power supply 218, which is a switching power regulator, has an intentionally limited slew rate, which is discussed below, increasing the possibility that this will occur.) When this occurs, power signal V_s will follow the envelope of output signal 232. However, due to the slow slew rate of main power supply 218 and the high slew rate of the output signal 232, output power signal V_s may not have any headroom between it and the envelope of output signal 232. In fact, output power signal V_s may be able to follow only the average of the envelope of output signal 232 and may actually be lower than output signal 232 at times, and may therefore be insufficient to power amplifier 204.

Please amend the paragraph beginning on page 13, line 16 as follows:

As mentioned above, frequency compensation block 214 increases the amplitude of frequency compensated signal 238 at higher frequencies. As a result, when higher frequencies are present in input signal 230, rectified signal 240 will be magnified in comparison to input signal 230, and therefore, control circuit 216 will regulate main power supply 218 to a higher target power level V_{targ} . If the increased amplitude of frequency compensated signal 238 at high frequencies is sufficient, then main power supply 218 may provide a sufficient power signal V_s to power amplifier 204.

Please amend the paragraph beginning on page 14, line 17 as follows:

Returning to a description of power amplifier 200, main power supply 218 will emit some electro-magnetic radiation, which produces electro-magnetic interference (EMI) in nearby electronic devices. As is well understood, the amount of EMI produced by a switching regulator such as main power supply 218 depends on its switching rate. In order to reduce EMI, the switching rate of

switch 246 is reduced by selecting a relatively low frequency for PWM control signal 242. The precise frequency chosen for PWM control signal 242 (which is a fixed frequency signal) will depend on the characteristics of load 234, output signal 232 and energy which must be delivered to properly power amplifier 204, among other criteria. A person skilled in the art will be capable of selecting a suitable frequency to balance these considerations with the need to reduce EMI emissions in a particular implementation of the present invention. Reducing the frequency of PWM control signal 242 and the switching rate of switch 246 has several effects.

Please amend the paragraph beginning on page 16, line 14 as follows:

Eventually, the magnitude of power signal V_s will rise to V_{targ} . At this point, power signal V_s will be sufficient to separately power amplifier 204. Until this time, it is necessary for switch 224 to keep transient power supply 223 engaged. The period for which switch 224 must remain in this state will depend on the slew rate of main power supply 218 and on the rate of change of input signal 230. The slew rate of main power supply 218 may be calculated (or more likely, the slew rate may be pre-determined based on the maximum EMI that power amplifier 200 is permitted to emit and then main power supply 218 may be designed to have the selected slew rate). Threshold 256 is selected to correspond to this slew rate, so that main power supply 223 will be kept engaged by switch 224 until power signal V_s is able to rise to V_{targ} .

Please amend the paragraph beginning on page 19, line 12 as follows:

Amplifier 235 is coupled to terminal 236 to receive power signal V_t and operates as in power amplifier 200 to produce reduced power signal V_{tr} . Summer 237 is coupled to rectifier 215 to receive rectified signal 240 and to amplifier 235 to receive reduced power signal V_{tr} and operates as in power amplifier 200 to produce error signal 239. Control circuit 284 receives control

signal 239 and produces an analog control signal 292, which is similar to control signal 244 of power amplifier 200. Switch 224 may couple control signal 292 to the gate of linear regulator 226, when transient power supply 223 is required to supply power signal V_i to amplifier 204, in the same manner as described above in relation to power amplifier 200. Power signals V_i and V_s are diode ~~or'd~~OR'd through diode 251 to produce power signal V_i .

Please amend the paragraph beginning on page 20, line 14 as follows:

Offset block 311a, frequency compensation block 314a and rectifier 315a, which comprise a first input signal compensation block 305a, are coupled to input terminal 302a in the same manner as offset block 211, frequency compensation block 214 and rectifier 215 are coupled to input terminal 202 of power amplifier 200. Rectifier 315a provides a rectified signal 340a corresponding to input signal 330a at terminal 341a. Similarly, offset block 311b, frequency compensation block 314b and rectifier 315b, which comprise a second input signal compensation block 305b, are coupled to input terminal 302b and rectifier 315b provides a rectified signal 340b corresponding to input signal 330b at terminal 341b. Terminals 341a and 341b are coupled to terminal 341 through diodes 360a and 360b. Rectified signals 340a and 340b are diode ~~or'd~~OR'd by diodes 360a and 360b, providing a rectified signal 340 at terminal 341, which corresponds generally to either the highest magnitude of signals 330a and 330b at any particular time. Offset blocks 311a and 311b may be configured to compensate for the diode drops caused by diodes 360a and 360b in rectified signals 340a and 340b.

Please amend the paragraph beginning on page 21, line 4 as follows:

Amplifier 304a is coupled to power input terminal 236 through an overload detect block 362a. Amplifier 304a receives power signal V_i and provides output signal 332a. Similarly amplifier 304b is coupled to power input terminal 236

through an overload detect block 362b and provides output signal 332b. Overload detect blocks 362a and 362b are configured to detect overload conditions in their associated amplifiers 304a and 304b. For example, overload detect blocks 362a and 362b may be configured to detect over-current, over-temperature or other overload conditions. If overload detect block 362a detects such a condition in its associated amplifier 304a, then overload detect block 362a will produce an overload signal 366a, which corresponds to the magnitude of the overload condition detected. Similarly, overload detect block 362b will produce an overload signal 366b if an overload is detected in amplifier 304b. Overload signals 366a and 366b are diode ~~or'd~~OR'd through diodes 364a and 364b to produce a combined overload signal 366, which is subtracted from rectified signal 340 to produce adjusted rectified signal ~~343~~370. Adjusted rectified signal ~~343~~370 is used to control the magnitude of power signal V_t . In this way, overload detect blocks 362a and 362b operate to reduce power signal V_t to protect amplifiers 304a and 304b when an overload occurs.

Please amend the paragraph beginning on page 21, line 21 as follows:

Since input signals 330a and 330b are independent of one another, they may have different magnitudes at any point in time. Accordingly, output signals 332a and 332b will have different amplitudes and amplifiers 304a and 304b will have different power requirements. Power signal V_t is large enough to power the amplifier 304a or 304b with the largest power requirement at any particular time (assuming that no overload condition exists). As a result, one of the amplifiers will receive more power than it requires and will dissipate the excess power.

Please amend the paragraph beginning on page 21, line 28 as follows:

It has been found that the dissipation of this excess power in one of the amplifiers 304a or 304b does not substantially reduce the average efficiency of power amplifier 300. Reference is made to Figure 5, which shows output signals

322a332a and 322b332b and power signal V_t . In the portion of the signals shown, output signal 322b332b is experiencing a peak at time t_1 . Output signal 322a is at a typical or average level. A typical audio signal, such as a movie soundtrack or music, may have a peak-to-average magnitude ratio of 8:1 or higher. At time t_1 , output signal 322a332a may have a current of 2 amps and a magnitude of 5 volts while output signal 322b332b may have a current of 14 amps and a magnitude of 35 volts. (Output signal 322b332b has 49 times more power than output signal 322a332a). Typically, output signal V_t may have an average magnitude of 41 volts (which is selected to account for any ripple in output signal V_t , to power the components of both amplifiers 204a and 204b and to provide reasonable headroom in the amplifier 204a or 204b with the higher power requirements) when amplifiers 304a and 304b are called on to produce these output signals 332a and 322b332b. Accordingly, output signal 322a332a has a headroom of 36 volts and will dissipate 72 watts of power (i.e. 36 volts x 2 amps). Output signal 322b332b has a headroom of 6 volts and will dissipate 84 watts (i.e. 6 volts x 14 amps). Amplifier 304b will therefore actually exhibit a high power loss, even though amplifier 304a has a much larger headroom. As a result, the large headroom created in amplifier 304a due to the peak of output signal 304b does not substantially increase the average power dissipated by power amplifier 300 in comparison to the power dissipated in amplifier 304b at the same time. Furthermore, peaks in a typical musical selection or a movie soundtrack occur relatively infrequently (and often occur on several channels simultaneously) and since the average level of a typical selection is generally less than 1/8th the level of the peaks in the selection, sharing main power supply 218 and transient power supply 223 between more than one amplifier does not result in a substantial change in the overall efficiency of power amplifier 300.

Please amend the paragraph beginning on page 24, line 20 as follows:

This is accomplished by using low voltage power supply 402 when the magnitude of output signal 232 is relatively small. Low voltage power supply 402

is coupled to positive power supply terminal 236 and provides a fixed voltage DC power signal V_{LV} to amplifier 204 at all times. Power signal V_{LV} is diode-~~or~~OR'd with power signal V_s and power signal V_t through diodes 404 and 251. In power amplifier 400, at any particular time, power signal V_t delivered to positive power input terminal 236 is equal to the highest of power signals V_t , V_s and V_{LV} .

Please amend the paragraph beginning on page 25, line 16 as follows:

Reference is made to Figure 7, which illustrates an average positive half wave of output signal 232 and power signal V_s , V_{LV} and V_t during the corresponding period. The magnitude V_{LV} of low voltage power supply 402 is selected to be a fraction of the average magnitude V_{s-avg} of power supply V_s during periods when output signal 232 is at an average level (i.e. a period during which no peaks occur). (During such periods, transient power supply 223 will generally not be engaged.) During the period shown in Figure 7, transient power supply 223 is disengaged. Between times t_2 and t_3 and between times t_4 and t_5 , the magnitude of output signal 232 is less than the magnitude of power signal V_{LV} and power signal V_t is equal to power signal V_{LV} . As noted above, control circuit 216 may be configured to disengage main power supply 418 is disengaged by setting control signal 442 to 0. In power amplifier 400, control circuit 416 is configured to disengage main power supply 418 when the magnitude of output signal 232 is less than a selected threshold V_d . When the magnitude of output signal 232 approaches threshold V_d , main power supply 418 is engaged by control circuit 416 to produce power signal V_s . Threshold V_d must be selected to ensure that main power supply 418 is engaged whenever power signal V_{LV} would be insufficient to power amplifier 204 to produce output signal 232. In selecting threshold V_d , the desired headroom (defined above as $V_{targ} - V_{req}$) must be taken into account. When main power supply 418 is engaged, power signal V_t will be equal to the higher of power signal V_{LV} and V_s .

Please amend the paragraph beginning on page 27, line 5 as follows:

Positive half circuit 508 is similar to positive half circuit 408 of power amplifier 400, except that control circuit ~~408~~416 has been replaced with a pulse density modulation (PDM) control circuit ~~508~~516 and main power supply 418 has been replaced with a main power supply 518 which is a resonant switching power regulator. Main power supply 518 may be any type of resonant switching regulator such as a zero-current-switching (ZCS) converter, a zero-voltage-switching (ZVS) converter, a zero-voltage-switching quasi-resonant converter (ZVS-QRC), a zero-voltage-switching multi-resonant converter (ZVS-MRC), a constant-frequency, a zero-voltage-switching quasi-resonant converter (CF-ZVS-MRC). Such converters are described in U.S. Patent 4,720,668, entitled "Zero Voltage Switching Quasi Resonant Converters" and in U.S. Patent 5,479,337, entitled "Very Low Power Loss Amplifier for Analog Signals Utilizing Constant-Frequency Zero-Voltage Switching Multi-Resonant Converter". Such regulators have the advantage of lower EMI emissions and lower switching losses than the non-resonant main power supplies 218, 318 and 418 described above in respect of power amplifiers 200, 280, 300 and 400.

Please amend the paragraph beginning on page 28, line 7 as follows:

Main power supply 518 receives PDM control signal 542 and produces a power signal V_{s-res} in response. Power signal V_{s-res} is analogous to power signal V_s produced by main power supply 218 of power amplifiers 200, 280, 300 and 400. Power signal V_{s-res} is ~~diode-OR'd~~OR'd with power signal V_i and V_{LV} to produce power signal V_t , which is received by amplifier 204 at terminal 236.

Please amend the paragraph beginning on page 28, line 30 as follows:

The constant on-time of PDM control signal 542 is selected to exceed time period t_8 , so that when switch 546 is opened at time t_7 (or later), switch 546 will essentially open a circuit which is carrying no current. During pulse 576,

capacitor 574 will have become charged, and when switch 546 is opened, capacitor 574 will have no voltage across it but will have a charge on it. After switch 546 is opened, this charge is discharged into filter 550. The minimum off-time of PDM control signal ~~546~~542 is selected to allow the charge on capacitor 574 to be essentially completely discharged. If the minimum off-time is too short, a charge will build up on capacitor 574 and the resonant operation of main power supply 518 will be degraded. The structure of PDM control circuit 516 is described below (Figure 11).

Please amend the paragraph beginning on page 29, line 9 as follows:

Reference is again made to Figure 8. As switch 546 opens and closes in response to PDM control signal 542, a series of pulses 576 are generated, forming a power signal V_{si-res} . LC filter 550 smooths power signal V_{si-res} to produce power signal V_{s-res} . The magnitude of power signal V_{s-res} during a particular time period will depend on the density of pulses 576 in power signal V_{si-res} . Power signal V_{s-res} is diode-~~or~~OR'd with power signal V_I and V_{LV} by diodes 251 and 404 to form power signal V_t , which is provided to power amplifier 204 at terminal 236.

Please amend the paragraph beginning on page 29, line 20 as follows:

Since PDM control signal 542 has a minimum off-time between each pulse ~~572~~576 (Figure 89), switch 546 cannot have a duty cycle of 100%. As a result, power signal V_{s-res} has a lower magnitude than the magnitude $V_{max-res}$ of power supply 512 (which is analogous to power source 212). To allow power signal V_{s-res} to have the same magnitude as power signal V_s of the power amplifiers described above, the magnitude $V_{max-res}$ of power supply 512 must be higher than the magnitude V_{max} of power source 212 (Figure 2).

Please amend the paragraph beginning on page 29, line 27 as follows:

Since each pulse 576 produced by switch 546 will be identical, each pulse 576 will transfer a fixed amount of energy first into capacitor 574 and then into filter 550. The magnitude of power signal V_{s-res} will depend entirely ~~efon~~ on the density of pulses 576 (i.e. on the variable off-time between pulses). When a low power signal V_{s-res} is required, the density of pulses 576 may be quite low and the frequency of the pulses may actually be in the audio band. Also, if the density of pulses is low, a large ripple may be seen in power signal V_{s-res} , and if filter 550 has a desirable low time constant (which allows power signal V_{s-res} to more closely follow the output signal 232, as described above in relation to power signal V_s of power amplifier 400), power signal V_{s-res} may also have a corresponding large ripple.

Please amend the paragraph beginning on page 32, line 18 as follows:

As noted above, positive half circuit 608 does not include low voltage power supply 402. In addition to regulating the level of power supply V_{t-reg} when an overload occurs, post regulator 684 also smooths power signal V_t so that power signal V_{t-reg} has less ripple than power signal V_t . As noted above in relation to power amplifier 400, one reason for using low voltage power supply 402 to eliminate the use of main power supply 218 (or resonant switching regulator 518) was to reduce ~~eliminate~~ the problem of a relatively large ripple on power signal V_t when power signal V_t had a relatively low magnitude. Since this ripple will be reduced by post regulator 684, the need for low voltage power supply 402 is reduced. If desired, low voltage power supply 402 may be incorporated into power amplifier 600 and a person skilled in the art will be capable of doing so.

Please amend the paragraph beginning on page 36, line 19 as follows:

In this way, rectified signal 240, power signal V_{t-reg} and overload detect signal 366 are used to generate error signal 239 and control signal 244. Switch 244224 operates in response to differential signal 254 to selectively couple control signal 244 to the gate of linear regulator 226 (Figures 3 and 10).

Please amend the paragraph beginning on page 37, line 19 as follows:

In an identical fashion, buffer B_2 produces a pulse 734 which remains high for a time t_{10} at terminal 730. Time t_{10} of pulse 734 will depend on the time constant of resistor R_{17} and capacitor C_5 . Diode D_5 D_4 provides a discharge path for capacitor C_5 when the Q output of buffer B_2 is low. In PDM control circuit 516, the values of resistors R_{16} and R_{17} and capacitors C_4 and C_5 are selected so that the time constant of resistor R_{17} and capacitor C_5 is shorter than the time constant of resistor R_{16} and capacitor C_4 . As a result, pulse 734 is shorter than pulse 732 (i.e. time t_{10} is shorter than time t_9).

Please amend the paragraph beginning on page 37, line 27 as follows:

The Q-not output of buffer B_1 is coupled to ground through resistor R_{18} and capacitor C_6 . The junction of resistor R_{18} and capacitor C_6 forms node 722, which is coupled to the second input of AND gate G_1 . When the Q-not output of buffer B_1 becomes high (at the end of pulse 732), resistor R_{18} and capacitor C_6 acts a delay circuit. After a time t_{11} , capacitor C_6 will be sufficiently charged so that node 722 is a high signal. After this time, AND gate will ~~re-initiate the~~ again provide a high signal to the clock inputs CLK of buffers B_1 and B_2 when error signal 239 is a high signal. This may occur immediately or may occur after some delay.

Please amend the paragraph beginning on page 38, line 4 as follows:

The inputs of AND gate G_2 are coupled to terminals 728 and 730 to receive pulses 732 and 734. The output of AND gate G_2 is coupled to terminal 241 to provide PDM control signal 542. As described earlier, PDM control signal 542 regulates the power signal V_{s-res} produced by main power supply 518. PDM control consists of a series of pulses which have a constant on-time (during which switch 546 (Figure 10) is closed, a minimum off-time following each pulse ~~following each pulse during which switch 546 must remain open~~ and a variable off-time between pulses which must exceed the minimum off-time and during which switch 546 remains open.

Please amend the paragraph beginning on page 40, line 12 as follows:

Power supply circuit 708 has two input signal compensation blocks 705a and 705b, which respectively comprise offset blocks 311a and 311b, frequency compensation blocks 314a and ~~315b~~314b and rectifiers 715a and 715b. In order to make power supply circuit 708 operative during positive and negative half waves of input signals 730a and 730b, rectifiers 315a and 315b of power amplifier 300 have been replaced with rectifiers 715a and 715b, which are full wave rectifiers and produce full wave rectified signals 740a and 740b which are ~~diode-or'd~~OR'd by diodes 360a and 360b to produce a full wave rectified signal 740 at terminal 341.

Please amend the paragraph beginning on page 42, line 13 as follows:

Amplifier circuit 804 comprises an op-amp 820, resistors 822, 824 and 826 and a capacitor 828. The negative input terminal of op-amp 820 is coupled to chassis ground 812 through resistor 822 and to the output of op-amp 820 through resistor 824. The positive input terminal of op-amp 820 is coupled to signal input terminal 802a through resistor 826. Signal input terminal 802a is coupled to chassis ground 812 through capacitor 828. Resistors 822 and 826 are selected to have a large and equal resistance. Resistor 824 is selected to

have a resistance much larger than that of resistor 822, thereby forming amplifier 804 into a non-inverting amplifying amplifier. Typically, resistors 822 and 826 may have a resistance of greater than 50 k Ω such as 100 k Ω or more and resistor 824 may have a resistance of 1 M Ω . With these values, amplifier 804 will operate as a multiply-by-10 amplifier. Preferably, amplifier 804 is configured to have an amplification of 2 to 20 times, and more preferably it will have a gain of 3 to 15 times.

Please amend the paragraph beginning on page 43, line 6 as follows:

EMI isolation circuit 800 reduces the coupling of EMI generated within positive half circuit 208 and negative half circuit 210 onto input signal 230 within power amplifier 230- as follows. Within the context of EMI isolation circuit 800, any such EMI may be seen as an EMI signal 835 across resistor 836, which is the only coupling between the floating power amplifier ground 814 and the chassis ground 812. Input signal 230 is received across terminal 802a and 802b. Input signal 230 is amplified by amplifier 804, which provides an amplified input signal 842 across nodes 840a and 840b corresponding to input signal 230. Input signal 230 combined with EMI signal 835 form an EMI contaminated input signal 846 across terminal 844a and 844b. EMI contaminated input signal 846 is reduced by amplifier 806, providing an EMI-decoupled input ~~830~~831 at terminal 202. This EMI-decoupled input signal ~~830~~831 is then amplified by power amplifier 200, as described above to produce output signal 232.

Please amend the paragraph beginning on page 43, line 19 as follows:

EMI-decoupled input signal ~~830~~831 will correspond substantially to input signal 230 with a relatively small degree of contamination from EMI signal ~~836~~835. This effect may be seen through the following example. If input signal 230 has a magnitude of 3 volts, EMI signal has a magnitude of -1, amplifier 804 has an amplification of 10 and amplifier 806 has an amplification of 0.1, then

amplified input signal 842 will have a magnitude of 30, EMI contaminated input signal 846 will have a magnitude of 29 and EMI-decoupled input signal ~~830~~831 will have a magnitude 2.9. By amplifying input signal 230 by a selected factor before it is contaminated by EMI signal 835 and then reducing EMI contaminated input signal 846 by the same factor, the effect of EMI signal 835 on input signal 230 is reduced by the selected factor, and consequently, the effect of EMI signal 835 on the operation of power amplifier 200 is reduced. It is not necessary that the amplification factor of amplifier 806 be the reciprocal of the amplification factor of amplifier 806. The amplification factors of amplifiers 804 and 806 may be varied to provide a desired degree of reduction of EMI signal 835 and an appropriate input signal for power amplifier 200.

Please amend the paragraph beginning on page 45, line 3 as follows:

When transient detect block 119 detects a change in input signal 130 that requires power amplifier 900 to enter transient operation, transient control circuit 923a generates a high pulse in transient control signal 904, which is OR'd with control signal 942 to produce a main power supply control signal 906. Main power supply control signal 906 is high when either control signal 142 or first transient control signal 904 is high. Control signal ~~942~~906 is a PWM signal similar to control signal 242 of power amplifier 200, and can have a duty cycle between 0 and 100%, depending on the value of compensated input signal 140. Main power supply 118 is responsive to main power supply control signal 906 and produces power signal V_s with a magnitude corresponding to main power supply control signal 906. When transient control signal 904 is low, main power supply control signal 906 is identical to control signal 142, and main power supply 118 provides power signal V_s as in power amplifier 100. When transient control signal 904 is high, main power supply control signal 906 will be high (i.e. it will have a duty cycle of 100%), and main power supply 118 will provide power signal V_s at its highest voltage.

Please amend the paragraph beginning on page 45, line 18 as follows:

When transient detect block 119 detects a change in input signal 130 that requires power amplifier 900 to enter transient operation, transient control circuit 923a~~b~~ also generates a low pulse on transient control signal 908. Transient control circuit 923b~~a~~ receives the low pulse and alters transient control signal 904 to increases the magnitude of error signal 939 in response to it. Control circuit 116 receives the increased error signal 939 and increases the duty cycle of control signal 142 in response. After a selected time, transient control circuit 923a ends the high pulse on transient control signal 904 and main power supply 118 becomes responsive to control signal 142. Main power supply 118 will provide power signal V_s with a voltage level corresponding to the increased duty cycle of control signal 142.

Please amend the paragraph beginning on page 45, line 28 as follows:

Transient control circuit 923b includes a fast attack block 910 and a slow release block 912. Fast attack block 910 operates to quickly increase the magnitude of error signal 939 in response to a low pulse on transient control signal 908. Slow release block 912 operates to slowly reduce the increase in error signal 939, until, after a selected time, transient control circuit 923b has no effect on error signal 939. Power amplifier 900 then returns to normal operation.

Please amend the paragraph beginning on page 47, line 1 as follows:

When transient signal 257 becomes high, power amplifier 1000 enters its transient operation. In response to transient signal 257 becoming high, one-shot circuit 1030 provides a high pulse 1034 on transient control signal ~~904~~1004, causing main power supply control signal 1006 to become high. Switch 246 of main power supply 218 remains closed while transient control signal ~~904~~1004 is

high, and main power supply 218 provides power signal V_s at its maximum voltage.

Please amend the paragraph beginning on page 47, line 29 as follows:

Diode 1040 is optional and may be provided to prevent current from flowing from node 1054 to node 1056 when capacitor 1042 is charged. Amplifier 1000 (like amplifiers 100, 200, 280, 300, 400, 500, 600, 700 and 900) uses a closed loop feedback through amplifier 235, summer 237 and control circuit 216 to reduce error signal 239 by keeping voltage V_{1056} approximately equal to the voltage V_{1060} of 1060 (to the extent possible, given the limits of main power supply 218). Amplifier 1052, resistor 1050 and 1046 provide an additional feedback loop, to enhance the control of error signal 239 and to keep voltages V_{1056} and V_{1060} approximately equal. Amplifier 1052, resistor 1050 and ~~1046~~1048 may be optionally provided in any of the amplifiers described above. In normal operation, capacitor 1044 will be discharged.

Please amend the paragraph beginning on page 48, line 8 as follows:

At time t_{12} , transient detect block 219 detects a large transient in the level of input signal 230 and sets transient signal 257 high. In response, one-shot circuit 1030 sets transient control signal 1004 high for a selected time period t_{13} and one-shot circuit 1032 sets transient control signal 1008 low for a selected time period t_{14} . Capacitor 1042 begins to discharge through diode 1038 into one-shot circuit 1032, causing voltage V_{1054} to fall. The low voltage of transient control signal 1008 is selected to sufficiently discharge capacitor 1042 so that the one-shot circuit 1032 begins to draw current from node 1056. For example, the low voltage of transient control signal 1008 may be selected to be ground, so that capacitor 1042 is fully discharged (assuming that the length of the low pulse is sufficiently long).

Please amend the paragraph beginning on page 49, line 20 as follows:

After time period t_{14} , transient control signal 1008 becomes high again. Capacitor 1054 begins to charge until voltage V_{1054} is equal to or higher than voltage V_{1056} (which will be a constantly varying voltage, depending on the magnitude of power signal V_t). If voltage V_{1056} subsequently exceeds V_{1054} , capacitor 1042 will again charge until voltage V_{1054} is equal to or higher than voltage V_{1056} .

In the Claims:

Please amend claims 1-3, 7-12, 16, 21-22, 27-30, 34-67, 70-71, 76, 82-85, 90, 96-98 as shown below.

1. (Amended) A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, said first output signal corresponding to said first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising:

- (a) a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level;
- (b) a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal;
- (c) a summer coupled to the first input signal compensation block and to the power signal compensation block for providing an error signal

corresponding to a difference between the target power level and the total power level of the total power signal;

- (d) a control circuit coupled to the summer for receiving the error signal and -for providing a first control signal and a second control signal in response to the error signal, wherein the first control signal corresponds to a target main power signal level and the second control signal corresponds to a target transient power signal level;
- (e) a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when the rate of change in the slew rate of the compensated input signal exceeds a selected transient threshold;
- (f) a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and
- (g) a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists;

wherein the control circuit provides the first and second control signals such that the target main power signal level is equal to or higher than the target transient power signal level and wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

2. (Amended) The power amplifier of claim 1 wherein the first input signal compensation circuitblock includes:

- (i) an offset block for adding an offset to said first input signal to provide an offset input signal;
- (ii) a frequency compensation block for receiving the offset input signal and for providing a corresponding frequency compensated

circuitsignal having its voltage components phase advanced with respect to its current component; and

- (iii) a first rectifier for rectifying the frequency compensated circuitsignal to provide the compensated input signal.

3. (Amended) The power amplifier of claim 2 wherein the frequency compensation block is configured to amplify the amplitude of selected the frequency compensated signal at selected frequency components, wherein said selected frequency components exceed a selected frequency compensation threshold.

7. (Amended) The power amplifier of claim 2 wherein the input-offset block is configured to add a smaller offset to the first input signal if the highest frequency component of the first input signal is less than a selected offset frequency threshold and to add a larger offset to the first input signal otherwise.

8. (Amended) The power amplifier of claim 1 wherein the first input signal compensation block provides the compensated input signal corresponding to a target power level that exceeds the sum of the power required by the first signal amplifier to generate a first output signal corresponding to the first input signal and at least half of a ripple in the main power signal.

9. (Amended) The power amplifier of claim 1 wherein the ~~first~~ control circuit is a PWM circuit-signal having a fixed switching frequency.

10. (Amended) The power amplifier of claim 9 wherein the main power supply is a switching regulator including:

- (i) a main power source;
- (ii) a switch coupled to the power source and responsive to the first control signal to provide an unfiltered main power signal; and

- (iii) an integrating filter coupled to the switch to provide the main power signal corresponding to the unfiltered main power signal.

11. (Amended) The power amplifier of claim 10 wherein the switching frequency is selected to limit the EMI emitted by the main power supply to a selected maximum EMI limit.

12. (Amended) The power supply of claim 10 wherein the transient detect block includes:

- (i) a peak detector for providing a peak signal corresponding to ~~the~~ peak envelope of the compensated input signal;
- (ii) a differentiator coupled to the peak detector for providing a differentiated signal corresponding to the rate of change of the compensated input signal; and
- (iii) a comparator for comparing the differentiated signal with the transient threshold to provide the transient signal;

and wherein the transient power supply includes:

- (iv) a transient power source;
- (v) a transient power regulator coupled to the control circuit for receiving the second control signal; and
- (~~iv~~vi) a transient supply switch for engaging the transient power regulator in response to the transient signal.

16. (Amended) The power amplifier of claim 11 wherein a time constant of the integrating filter is selected to effectively smooth the main power signal compared to the unfiltered main power signal.

21. (Amended) The power amplifier of claim 1 wherein a second signal amplifier is coupled to the first power terminal and a second input signal is received at a second input terminal and wherein the first input signal

compensation block provides a first compensated input signal and further including:

- (i) a second input signal compensation block for providing a second compensated input signal; and
- (ii) a ~~combining~~magnitude comparing circuit for ~~combining~~comparing the first and second compensated input signals ~~to~~and ~~provide~~ing the compensated input signal ~~having~~with a magnitude corresponding to the higher magnitude of the first and second compensated input signals.

22. (Amended) The power amplifier of claim 21 wherein the ~~combining~~magnitude comparing -circuit is a pair of diodes ~~for diode OR'ing~~ wherein the first and second compensated input signals are diode OR'd for generating the compensated input signal.

27. (Amended) The power amplifier of claim 23 further including a post regulation circuit having:

- (i) an overload detect block coupled to the first signal amplifier to provide an overload signal corresponding to one or more overload conditions within the first signal amplifier;
- (ii) a second rectifier coupled to the offset block for receiving the offset input signal and providing a rectified input signal;
- (iii) a third summer for subtracting the overload signal from the rectified input signal to provide a regulation signal;
- (iv) a regulation amplifier coupled to the third summer for providing an amplified regulation signal corresponding to the regulation signal and having a magnitude range corresponding to the magnitude range of the total power signal;
- (v) a post regulator having a control terminal, and coupled between the main and transient power supplies and the first power terminal; and

- (vi) a regulation feedback circuit coupled between the first power terminal and the control terminal of the post regulator and including a fourth summer for providing a regulator error signal corresponding to the difference between the total power signal and the amplified regulation signal;

wherein the post regulator regulates the total power signal in response to the regulator error signal when an overload condition occurs.

28. (Amended) The power amplifier of any one of claims 2-5 or 7-27 wherein the first signal amplifier is a bridge amplifier and wherein the first rectifier is a full wave rectifier.

29. (Amended) The power amplifier of any of claims 1-27 wherein the first signal amplifier has a second power terminal and further including a second power supply circuit having the same structure as said first power supply circuit, wherein said first power supply circuit supplies power to said first signal amplifier at said first power terminal during positive half wave of said first output signal and said second power supply circuit provides power to said first signal amplifier at said second power terminal during negative half waves of said first output signal.

30. (Amended) The power amplifier of claim 1 further including an EMI isolation circuit coupled between said first input terminal and an internal input terminal for providing a first EMI-decoupled signal corresponding to said first input signal at said internal input terminal, and wherein said first input signal compensation block and said first signal amplifier are coupled to said internal input ~~node~~terminal, wherein the EMI isolation circuit has:

- (i) a first isolation amplifier having a first amplification factor coupled to said first input terminal through a first impedance for receiving said first input signal and for providing an amplified input signal; and
- (ii) a second isolation amplifier having a second amplification factor coupled to said first amplifier for receiving said amplified input

signal and to said internal input terminal for providing said first EMI-decoupled signal;

wherein the first amplification factor of the first isolation amplifier is greater than 1 and the second amplification factor of said second isolation amplifier is less than 1.

34. (Amended) A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, said first output signal corresponding to said first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising:

- (a) a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level;
- (b) a power signal compensation block for receiving the total power signal and for providing a compensated power signal corresponding to the total power signal;
- (c) a summer coupled to the first input signal compensation block and to the power signal compensation block for providing an error signal corresponding to a difference between the target power level and the power level of the total power signal;
- (d) a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when the a rate of change in the a slew rate of the compensated input signal exceeds a selected transient threshold;
- (e) a first transient control circuit coupled to the transient detect block for providing first and second digital transient control signals;

wherein the first digital transient control signal indicates the occurrence of a transient condition for a first time period in response to the transient signal and wherein the second digital transient control signal indicates the occurrence of a transient condition for a second time period in response to the transient signal, and wherein the second time period is longer than the first time period;

- (f) a control circuit coupled to the summer for receiving an amplified error signal for providing a first control signal in response to the amplified error signal;
- (g) a signal combining block for combining the first control signal and the first transient control signal to provide a main power supply control signal;
- (h) a selectively engageable second transient control circuit coupled to the first transient control signal circuit for receiving the second digital transient control circuit signal and for temporarily increasing the magnitude of the error signal, wherein the second transient control circuit is engaged and disengaged—in response to the second digital transient control signal, the second transient control circuit including a feedback amplifier coupled between the summer and the control circuit to provide the amplified error signal, the feedback amplifier being operative at all times; and
- (i) a main power supply for providing a main power signal at the first power terminal in response to the main power supply control signal;

wherein the total power signal corresponds to the main power signal.

35. (Amended) The first power supply circuit of claim 34 wherein the first transient control circuit includes a first one-shot circuit for generating the first digital transient control signal, wherein the first one-shot circuit is triggered by the transient signal indicating the occurrence of a transient condition.

36. (Amended) The first power supply circuit of claim 35 wherein the first transient control circuit includes a second one-shot circuit for generating the second digital transient control signal, wherein the second one-shot is triggered by the transient signal indicating the occurrence of a transient condition.

37. (Amended) The first power supply circuit of claim 36 wherein the second transient control circuit includes:

- (i) a fast ~~release~~attack block for initially increasing the error signal rapidly when the second transient control circuit becomes engaged; and
- (ii) a slow release block for slowly reducing the increase in the error signal.

38. (Amended) The first power supply circuit of claim 37 wherein the first time period is selected to be longer than the time required for the fast attack block to increase the magnitude of the error signal.

39. (Amended) The first power supply circuit of claim 37 wherein the second transient control circuit comprises:

- (i) a first diode having its cathode coupled to the output of the second one-shot circuit and having its anode coupled to a first node;
- (ii) a first capacitor coupled between the first node and ground;
- (iii) a first resistor and a second capacitor coupled in parallel between the first node and a second node, wherein the second node is coupled to a third node at the coupling of the summer and the power signal compensation block; and
- (iv) a feedback network including a second resistor and a third capacitor coupled between the third node and a fourth node at the coupling of the feedback amplifier and the control circuit.

40. (Amended) The first power supply circuit of claim 39 wherein:

- (i) the second digital transient control signal is normally high in the absence of a transient condition and becomes low when the second one-shot is triggered;
- (ii) the first capacitor is normally charged in the absence of a transient condition and is discharged through the first diode when the second one-shot is triggered; and
- (iii) the first and second resistances act as a voltage divider in response to the discharging of the first capacitor to initially increase the magnitude of the amplified error signal.

41. (Amended) The first power supply circuit of claim 37 wherein the signal combining block includes an OR gate.

42. (Amended) The first power supply circuit of claim 39 wherein the first input compensation ~~circuit~~block includes:

- (i) an offset block for adding an offset to said first input signal to provide an offset input signal;
- (ii) a frequency compensation block for receiving the offset input signal and for providing a corresponding frequency compensated ~~circuit~~signal having its voltage components phase advanced with respect to its current component; and
- (iii) a first rectifier for rectifying the frequency compensated ~~circuit~~signal to provide the compensated input signal.

43. (Amended) The first power supply circuit of claim 42 wherein the frequency compensation block is configured to amplify the amplitude of selected the frequency compensated signal at selected frequency components, wherein said selected frequencies exceed a selected frequency compensation threshold.

44. (Amended) The first power supply circuit of claim 43 wherein the amplitude of the selected frequency components is progressively amplified to a greater extent.

45. (Amended) The first power supply circuit of claim 43 wherein the amplitude of the selected frequency components is equally amplified.

46. (Amended) The first power supply circuit of claim 42 wherein the first rectifier is a half wave rectifier.

47. (Amended) The first power supply circuit of claim 42 wherein the input offset block is configured to add a smaller offset to the first input signal if the highest frequency component of the first input signal is less than a selected offset frequency threshold and to add a larger offset to the first input signal otherwise.

48. (Amended) The first power supply circuit of claim 42 wherein the first input signal compensation block provides the compensated input signal corresponding to a target power level that exceeds the sum of the power required by the first signal amplifier to generate a first output signal corresponding to the first input signal and at least half of a ripple in the main power signal.

49. (Amended) The first power supply circuit of claim 40 wherein the first control circuit is a PWM signal having a fixed switching frequency.

50. (Amended) The first power supply circuit of claim 39 wherein the main power supply is a switching regulator including:

- (i) a main power source;
- (ii) a switch coupled to the main power source and responsive to the first control signal to provide an unfiltered main power signal; and
- (iii) an integrating filter coupled to switch to provide the main power signal corresponding to the unfiltered main power signal.

51. (Amended) The first power supply circuit of claim 50 wherein the a switching frequency is selected to limit the EMI emitted by the main power supply to a selected maximum EMI limit.

52. (Amended) The first power supply of claim 50 wherein the transient detect block includes:

- (i) a peak detector for providing a peak signal corresponding to the a peak envelope of the compensated input signal;
- (ii) a differentiator coupled to the peak detector for providing a differentiated signal corresponding to the a rate of change of the compensated input signal; and
- (iii) a comparator for comparing the differentiated signal with the transient threshold to provide the transient signal.

53. (Amended) The first power supply circuit of claim 51 wherein a time constant of the integrating filter is selected to effectively smooth the main power signal compared to the unfiltered main power signal.

54. (Amended) The first power supply circuit of claim 52 wherein a discharge rate of the peak detector is selected to correspond to a slew rate of the main power supply.

55. (Amended) The first power supply circuit of claim 40 further including:

- (i) an overload detect block coupled to the first signal amplifier to provide an overload signal corresponding to one or more overload conditions within the first signal amplifier; and
- (ii) means for combining the overload signal with the compensated input signal to provide an adjusted compensated input signal;

wherein the error signal corresponds to a difference between the adjusted compensated input signal and compensated power signal.

56. (Amended) The first power supply circuit of claim 55 wherein the means for combining is the summer.

57. (Amended) The first power supply circuit of claim 55 wherein the means for combining is a second summer.

58. (Amended) The first power supply circuit of claim 40 wherein a second signal amplifier is coupled to the first power terminal and a second input signal is received at a second input terminal and wherein the first input signal compensation block provides a first compensated input signal and further including:

- (i) a second input signal compensation ~~from~~block for providing a second compensated input signal; and
- (ii) a ~~combining circuit~~magnitude comparing circuit for ~~combining~~comparing the first and second compensated input signals ~~to~~and provideing the compensated input signal ~~having with~~ a magnitude corresponding to the higher of the first and second compensated input signals.

59. (Amended) The first power supply circuit of claim 58 wherein the ~~combining~~magnitude comparing circuit is a pair of diodes ~~for diode OR'ing~~ wherein the first and second compensated input signals are diode OR'd for generating the compensated input signal.

60. (Amended) The first power supply circuit of claim 40 wherein the first control signal is a pulse density modulated control signal and wherein the main power supply is a resonant switching power regulator.

61. (Amended) The first power supply circuit of claim 60 wherein the main power supply is a zero-current switching regulator and includes an LC resonant tank.

62. (Amended) The first power supply circuit of claim 40 further including a low voltage power supply coupled for providing a fixed low voltage power signal to the first power terminal, wherein the total power signal is generally equal to the higher of the magnitude of the main power signal, the magnitude of the transient power signal or the magnitude of the low voltage power signal.

63. (Amended) The first power supply circuit of claim 62 wherein the control circuit is configured to set the main power signal to zero when the target power level is less than the magnitude of the low voltage power signal.

64. (Amended) The first power supply circuit of claim 60 further including a post regulation circuit having:

- (i) an overload detect block coupled to the first signal amplifier to provide an overload signal corresponding to one or more overload conditions within the first signal amplifier;
- (ii) a second rectifier coupled to the offset block for receiving the offset input signal and providing a rectified input signal;
- (iii) a third summer for subtracting the overload signal from the rectified input signal to provide a regulation signal;
- (iv) a regulation amplifier coupled to the third summer for providing an amplified regulation signal corresponding to the regulation signal and having a magnitude range corresponding to the magnitude range of the total power signal;
- (v) a post regulator having a control terminal, and coupled between the main and transient power supplies and the first power terminal; and
- (vi) a regulation feedback circuit coupled between the first power terminal and the control terminal of the post regulator and including

a fourth summer for providing a regulator error signal corresponding to the difference between the total power signal and the amplified regulation signal;

wherein the post regulator regulates the total power signal in response to the regulator error signal when an overload condition occurs.

65. (Amended) The first power supply circuit of any one of claims 40-45 or 47-64 wherein the first signal amplifier is a bridge amplifier and wherein the first rectifier is a full wave rectifier.

66. (Amended) The power amplifier of any of claims 40-64 wherein the first signal amplifier has a second power terminal and further including a second power supply circuit having the same structure as said first power supply circuit, wherein said first power supply circuit supplies power to said first signal amplifier at said first power terminal during positive half wave of said first output signal and said second power supply circuit provides power to said first signal amplifier at said second power terminal during negative half waves of said first output signal.

67. (Amended) The power amplifier of claim 34 further including an EMI isolation circuit coupled between said first input terminal and an internal input terminal for providing a first EMI-decoupled signal corresponding to said first input signal at said internal input terminal, and wherein said first input signal compensation block and said first signal amplifier are coupled to said internal input ~~node~~terminal, wherein the EMI isolation circuit has:

- (i) a first isolation amplifier having a first amplification factor coupled to said first input terminal through a first impedance for receiving said first input signal and for providing an amplified input signal; and
- (ii) a second isolation amplifier having a second amplification factor coupled to said first amplifier for receiving said amplified input signal and to said internal input terminal for providing said first EMI-decoupled signal;

wherein the first amplification factor of the first isolation amplifier is greater than 1 and the second amplification factor of said second isolation amplifier is less than 1.

70. (Amended) A method of supplying a total power signal to a signal amplifier, comprising:

- (a) receiving an input signal;
- (b) producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target power level for the total power signal;
- (c) comparing the compensated input signal to a reduced version of the total power signal to produce an error signal;
- (d) providing first and second control signals in response to the error signal;
- (e) providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal;
- (f) comparing ~~the~~a rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the transient threshold, the transient threshold corresponding to ~~the~~a maximum slew rate of the main power ~~supply~~signal; and
- (g) engaging a transient power supply to provide a transient power signal in response to said second control signal, when the transient signal indicates ~~a~~the transient condition, the transient power signal being a second part of the total power signal.

71. (Amended) The method of claim 70 wherein step (b) includes:

- (i) adding an offset to the input signal;

- (ii) amplifying frequency components of the input signal exceeding a selected threshold frequency; and
- (iii) rectifying the result of step (b).

76. (Amended) The method of claim 70 further including providing an overload signal corresponding to an overload condition in the signal amplifier and reducing the magnitude of the main power signal in response to the overload signal.

82. (Amended) The method of claim 81 further including providing an overload signal corresponding to an overload condition in the signal amplifier and reducing the magnitude of the total power signal in response to the overload signal.

83. (Amended) The method of claim 71 wherein the signal amplifier is a bridge amplifier and step (iii) is performed by full wave rectifying the result of step (ii).

84. (Amended) A method of supplying a total power signal to a signal amplifier, comprising:

- (a) receiving an input signal;
- (b) producing a compensated input signal corresponding to the input signal, the compensated input signal defining a target power level for the total power signal;
- (c) comparing the compensated input signal to a reduced version of the total power signal to produce an error signal;
- (d) providing first and second control signals in response to the error signal;
- (e) providing a main power signal using a switching regulator in response to the first control signal, the main power signal being a first part of the total power signal;

- (f) comparing the rate of change of the compensated input signal to a selected transient threshold to provide a transient signal, the transient signal identifying a transient condition when the rate of change exceeds the transient threshold, the transient threshold corresponding to the maximum slew rate of the main power supply signal; and
- (g) in response to a transient condition, temporarily engaging the switching regulator with a 100% duty cycle for a first time period and temporarily elevating the error signal for a second time period.

85. (Amended) The method of claim 84 wherein step (b) includes:

- (i) adding an offset to the input signal;
- (ii) amplifying frequency components of the input signal exceeding a selected threshold frequency; and
- (iii) rectifying the result of step (b).

90. (Amended) The method of claim 84 further including providing an overload signal corresponding to an overload condition in the signal amplifier and reducing the magnitude of the main power signal in response to the overload signal.

96. (Amended) The method of claim 95 further including providing an overload signal corresponding to an overload condition in the signal amplifier and reducing the magnitude of the total power signal in response to the overload signal.

97. (Amended) The method of claim 85 wherein the signal amplifier is a bridge amplifier and step (iii) is performed by full wave rectifying the result of step (ii).

98. (Amended) A power amplifier for receiving a first input signal at a first input terminal and for producing a first output signal at a first output terminal, said first output signal corresponding to said first input signal, a first signal amplifier being coupled to the first input terminal to receive the first input signal and coupled to the first output terminal to provide the first output signal, the first signal amplifier having a first power terminal for receiving a total power signal and said power amplifier having a first power supply circuit comprising:

- (a) a first input signal compensation block coupled to the first input terminal to receive the first input signal and to provide a compensated input signal corresponding to the first input signal, wherein the compensated input signal defines a target power level;
- (b) a main power signal compensation block for receiving a main power signal and for providing a compensated main power signal corresponding to the main power signal;
- (c) a first summer coupled to the first input signal compensation block and to the main power signal compensation block for providing a first error signal corresponding to a difference between the target power level and ~~the~~a power level of the main power signal;
- (d) a first control circuit coupled to the first summer for receiving the first error signal and for providing a first control signal in response to the ~~second~~first error signal, wherein the first control signal corresponds to a target main power signal level;
- (e) a total power signal compensation block for receiving the total power signal and for providing a compensated total power signal corresponding to the total power signal;
- (f) a second summer coupled to the first input signal compensation block and to the total power signal compensation block for providing ~~a~~the second error signal corresponding to a difference between the target power level and ~~the~~a power level of the total power signal;

- (g) a second control circuit coupled to the second summer for receiving the second error signal and for providing a second control signal in response to the second error signal, wherein the second control signal corresponds to a target transient power signal level;
- (h) a transient detect block coupled to the first input signal compensation block for providing a transient signal to identify a transient condition when the a rate of change in the a slew rate of the compensated input signal exceeds a selected transient threshold;
- (i) a main power supply for providing a main power signal at the first power terminal in response to the first control signal; and
- (j) a selectively engageable transient power supply for providing a transient power signal at the first power terminal in response to the second control signal and the transient signal, wherein the transient power supply is engaged when the transient signal indicates that a transient condition exists;

wherein the magnitude of the total power signal is generally equal to the higher of the magnitude of the main power signal or the magnitude of the transient power signal.

MARKED UP VERSION

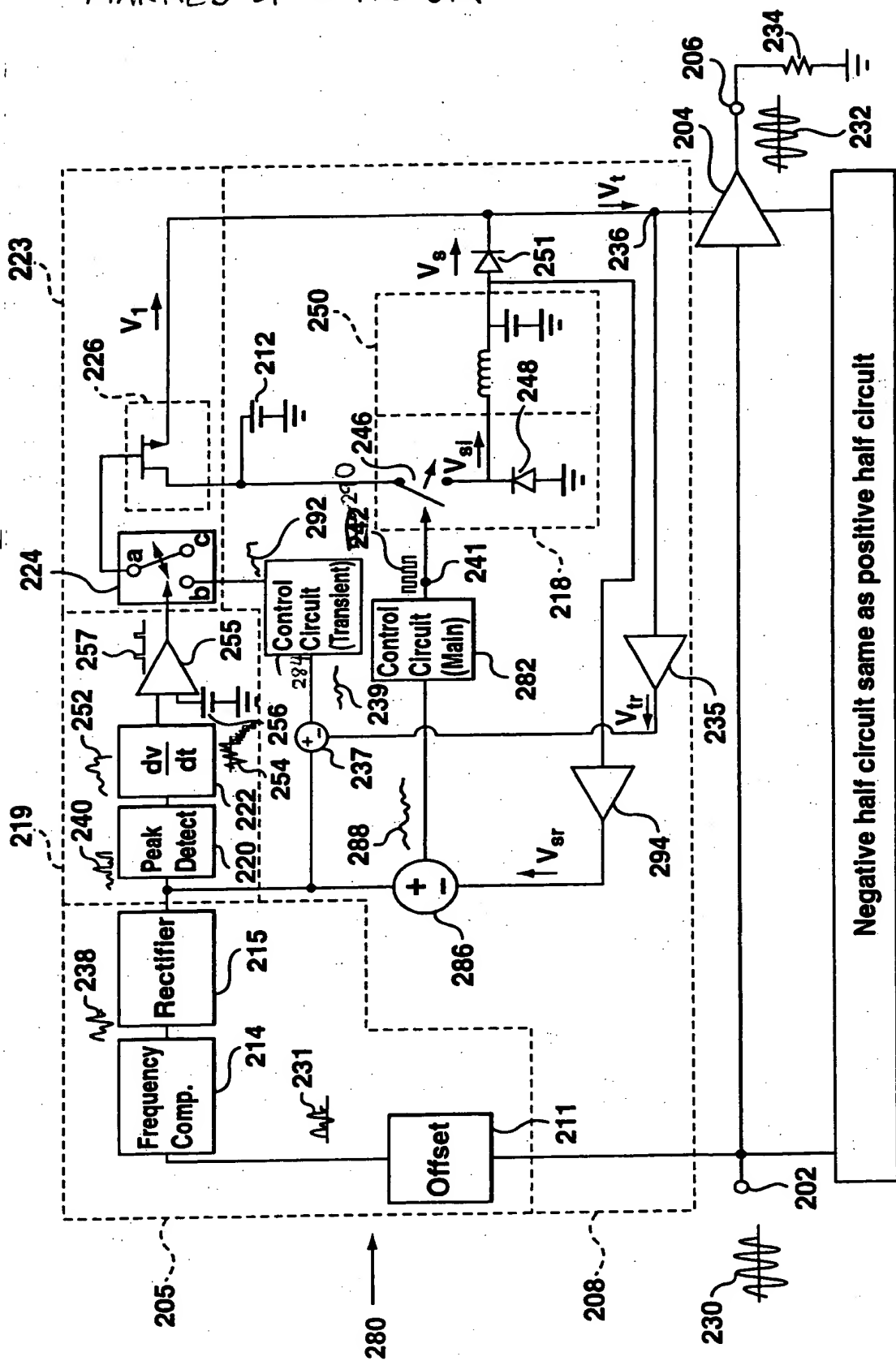


FIG. 3

MARKED-UP VERSION

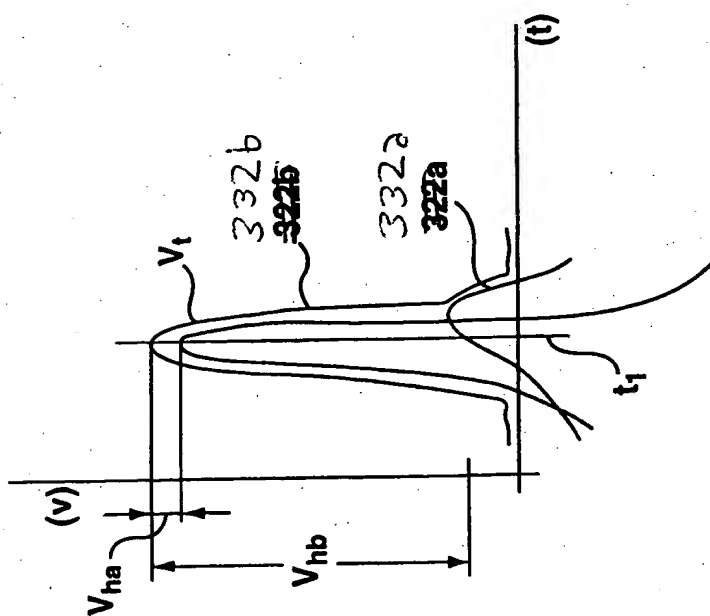


FIG. 5

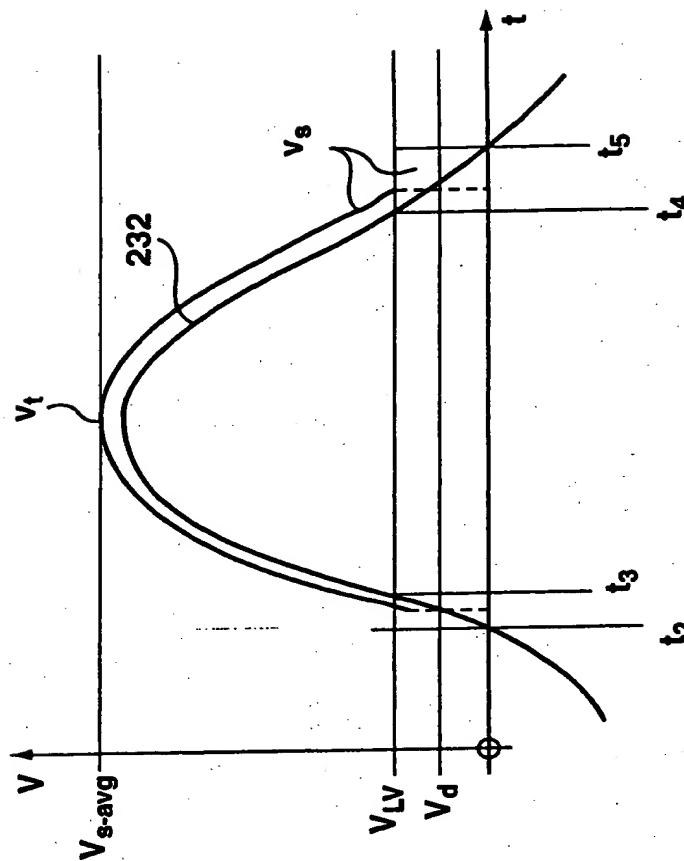


FIG. 7

MARKED-UP VERSION

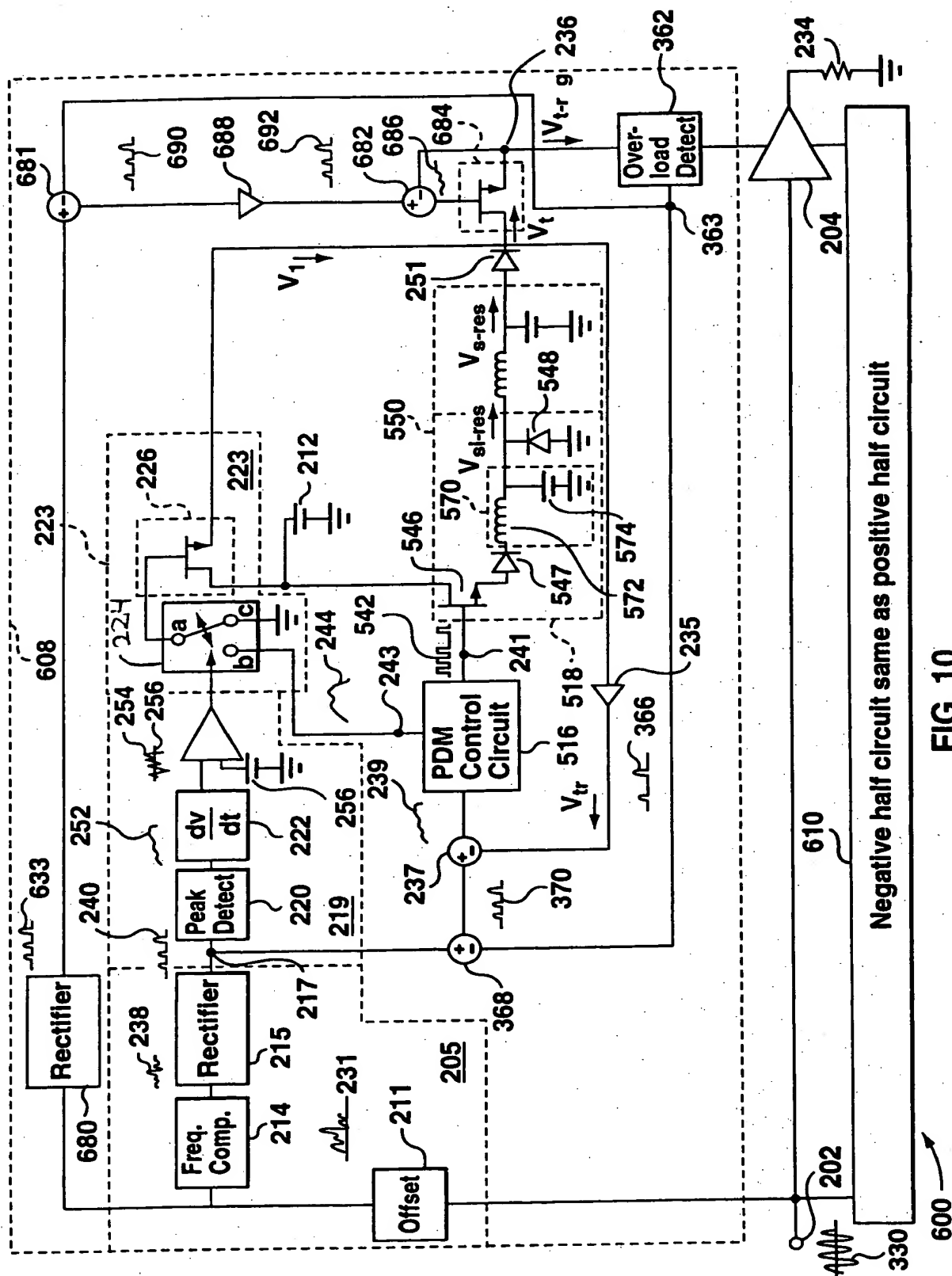


FIG. 10

MARKED UP VERSION



FIG. 11

MARKED UP
VERSION

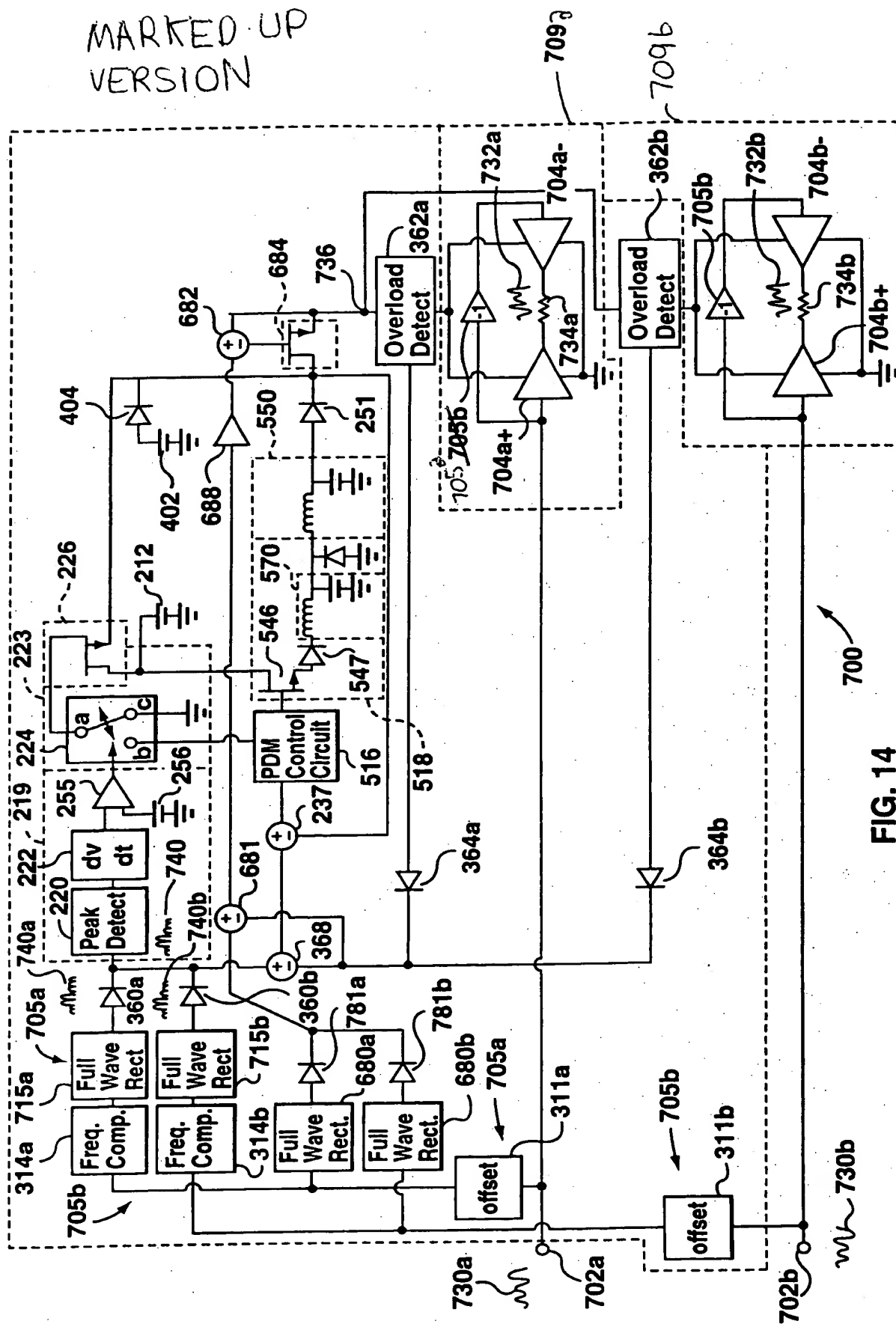


FIG. 14

MARKED UP VERSION

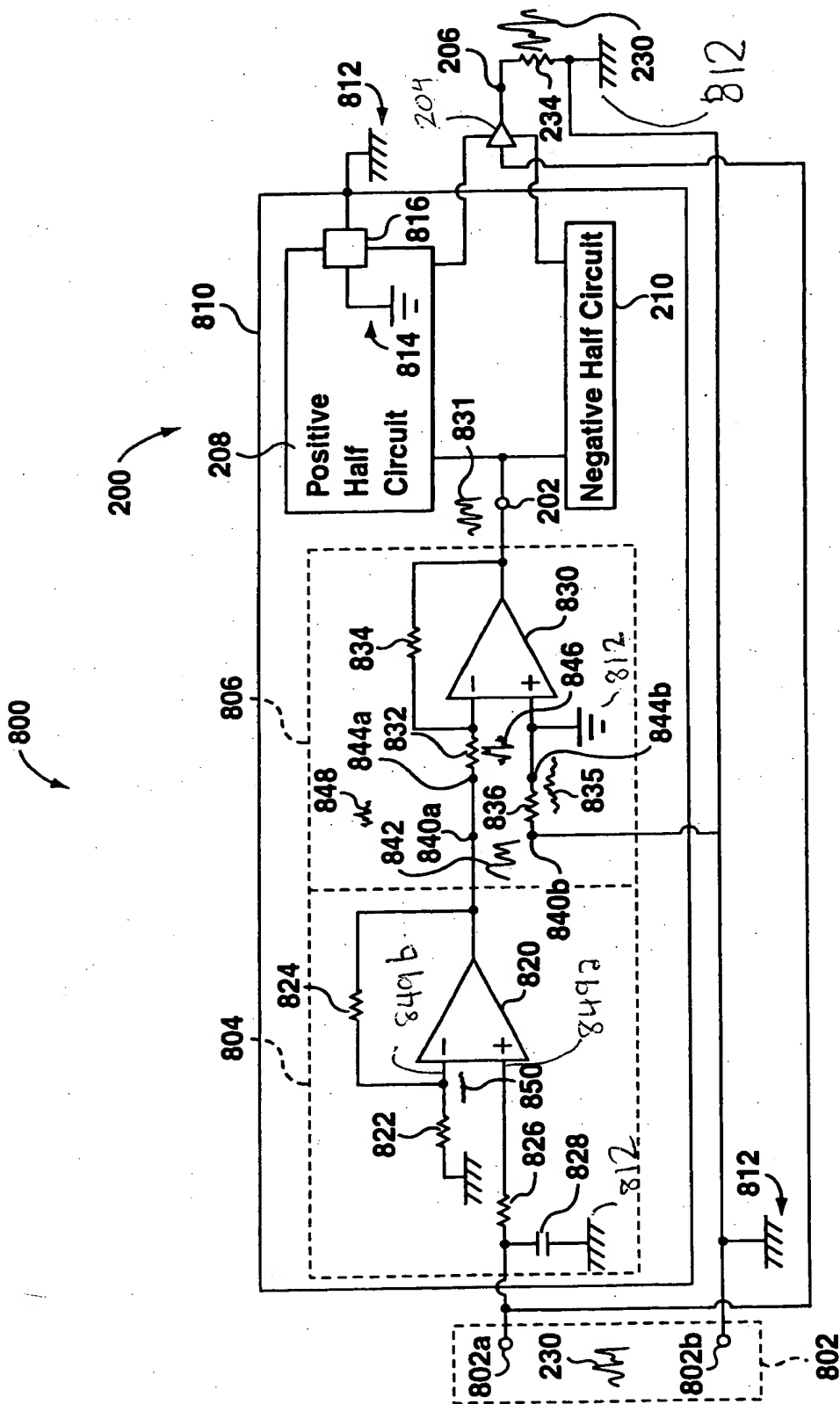


FIG. 15

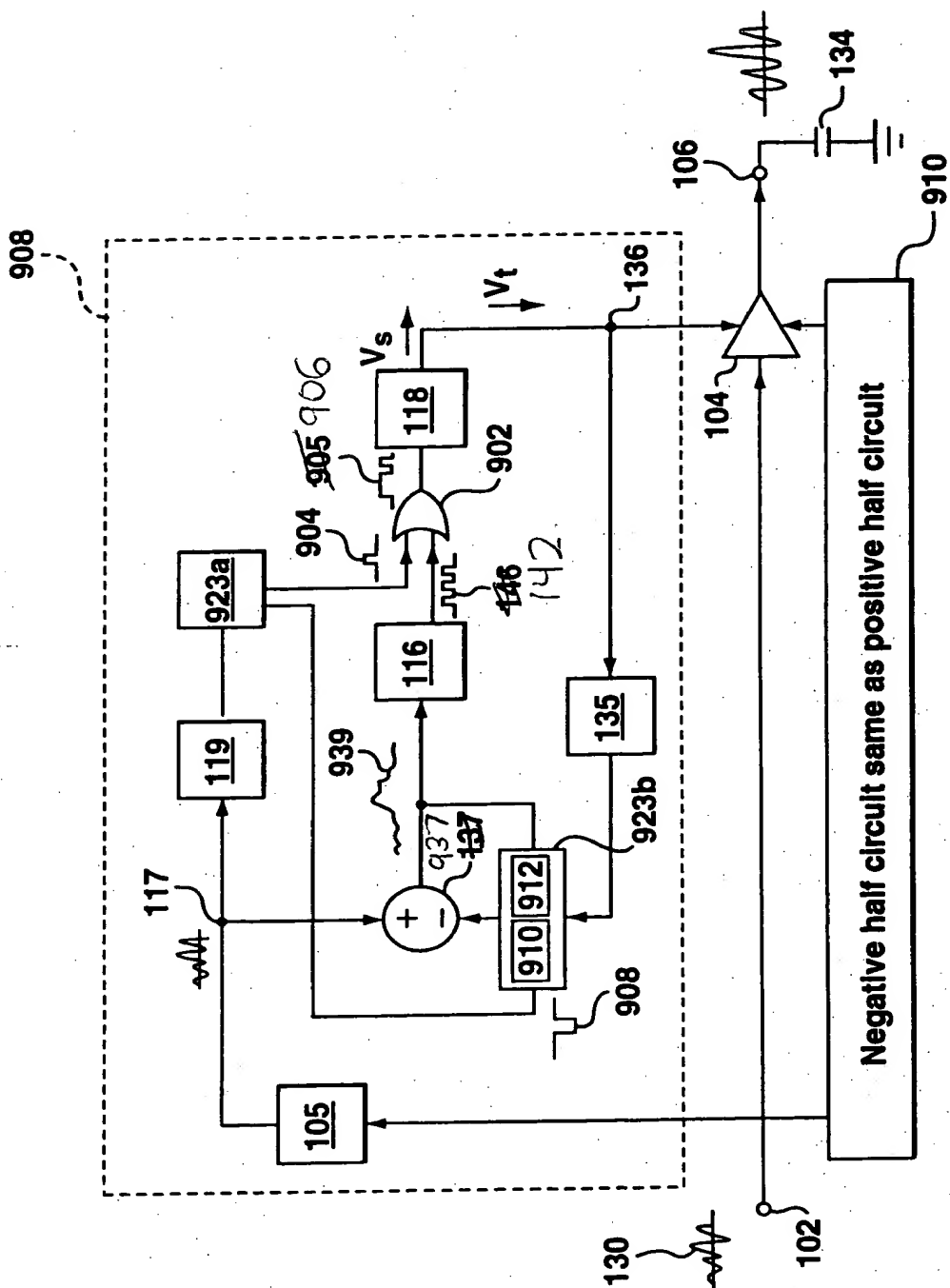


FIG. 16

